Efficient FPGA Based Subtractive Synthesis Implementation

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Abstract

In the past few decades musical sound synthesis has moved from analog domain to digital and software domains. Within many methods of sound synthesis, many portions of the signal can be processed independently of each other. In this case the signal could be assembled through many parallel calculations. For analog and digital domains this is a natural flow. This parallelization is particularly applicable to the subtractive sound synthesis algorithm being researched.

This research is being done to analyse the performance gains of rewriting a software subtractive synthesis algorithm onto a Field Programmable Gate Array (FPGA). The used FPGA will be the Cyclone II on the Altera DE1 board. The primary reason the specific algorithm was chosen was observed real-time performance issues when implemented in software, along with its musical characteristics.