A Physics-Based Thermal Circuit Model for FinFETs

by

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A Thesis Proposal by

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Abstract/Executive Summary

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Abstract

The Complementary metal-oxide-semiconductor (CMOS) device has been rapidly evolving and its size has been drastically decreasing ever since it was first fabricated in 1960 [Us Patent 3,356,858: 1967]. The substantial reduction in the CMOS device size has led to short channel effects which have resulted in the introduction of SOI technology that has allowed Moore’s Law to continue to predict the evolution of microelectronics technology. Moore’s law was proposed by Gordon Moore who predicted in 1965 that the number of semiconductor devices in a chip is doubled every 18 to 24 months [1]. While device dimensions continue decreasing, conventional planar transistors have reached feasible size limits due to undesirable short-channel effects, which lead to poor device performance. The effort to overcome these has given rise to the creation of multi-gate field effect transistors (MUGFETS). A specific type of the MUGFET is known as the Fin Field Effect Transistor (FinFET), which is a non-planar, tri-gate transistor built on a silicon on insulator (SOI) substrate.

The desire to continue scaling down CMOS device dimensions resulted in the introduction of SOI technology, which however, has enhanced the self-heating issues in CMOS technology due to the low-thermal conductive buried oxide (BOX) that was placed between the active device and the silicon substrate. Furthermore, due to the geometry of the FinFET the severity of the heating problem has dramatically increased. Self-heating in the 3-dimensional FinFET device enhances the temperature gradients and peak temperature, which decrease drive current, increase the interconnect delays and degrade the device and interconnect reliability. Also, the leakage power depends exponentially on the temperature. It is therefore crucial for chip designers to consider thermal influences on device/interconnect/chip performance and their reliability. A typical Integrated Circuit (IC) chip however consists of millions of transistors, making direct numerical simulation impractical. Accurate thermal models for the FinFET that is detailed enough to provide the device temperature profile and efficient enough for large scale electro-thermal simulation are therefore strongly desirable.

The proposed thesis aims to develop an accurate thermal model for the FinFET through a rigorous physics-based mathematical approach. From this approach we expect to account for non-isothermal effects along the fin. A thermal circuit for the FinFET will be derived from the model, and the developed thermal circuit will then be implemented in a circuit simulator, such as Spice, for efficient and accurate electro-thermal simulation. The thermal solution derived from this approach will be validated against finite element simulations. This approach accounting for the non-uniform thermal profile along the device is able to provide more accurate simulation of heat flow to interconnects; allowing chip designers to predict interconnect temperature. The capability of self-consistent electro-thermal simulation in a Spice simulator offers an efficient tool for chip design to take into account thermal effects on electronic performance and reliability of devices and chips to achieve cost-effective design for the FinFET-based semiconductor chips.
1. Introduction

A vast majority of integrated circuits are produced in CMOS technology. These devices are based on a pair of complementary MOSFETs including n-channel and p-channel field effect transistors. The n-channel device employs a sufficiently high positive voltage to the gate with respect to the source, and electrons are then attracted to the semiconductor surface to establish a conductive n-channel between the source and drain, making current flow possible. The gate voltage necessary to form the channel is called the threshold voltage \( (V_T) \). However, the p-channel device requires a negative gate voltage for a conductive p-channel. Over the past 15 years, there has been a new CMOS technology node introduced (meaning the device length and metal width are further scaled down) approximately every two years. The number of devices in a single chip is approximately doubled, and the number density of devices has been significantly increased. Thus, the power density has been increasing rapidly, approaching air cool limit. The transistor channel length has decreased almost 3 orders of magnitude in approximately 30 years. However, the reduction of horizontal dimensions (such as gate length and metal width) must be accompanied by an appropriate reduction of vertical ones (such as oxide gate thickness and device channel thickness), as well as increased doping and lowered supply voltage [2]. The negative effects of failing to meet these criteria will be explained in greater detail later in this proposal.

![Figure 1 (a) Bulk CMOS and (b) SOI CMOS structures [3]](image)

The most popular microelectronics technology is based on the conventional bulk CMOS structure shown in Figure 1(a) where the device is placed directly on a bulk silicon substrate. Bulk CMOS devices however suffer from large parasitic capacitances and pronounced short channel effects because of the bulk silicon. In particular, the short-channel effect is one of the vital issues in the fast growing semiconductor industry and will be explained in more detail later. An additional issue of BULK CMOS is caused by latch-up due to the n-well or p-well structure used to isolate the device, which may actually lead to a short circuit between n-channel and p-channel devices. These issues are substantially minimized with the introduction of SOI technology whose n-channel MOSFET structure is shown in Figure 1(b). Unlike the conventional MOSFET technology, a layer of buried oxide (BOX) is placed between the thin
silicon island, where the active device is, and the silicon substrate, as illustrated in Figure 1 (b). The BOX layer effectively reduces the parasitic capacitance, diminishes short channel effects and resolves the latch-up issues in the conventional CMOS technology.

In SOI technology, the isolation of the device from the bulk substrate is the key in solving the problems faced by the bulk CMOS devices. This gives (SOI) CMOS structures numerous advantages over bulk CMOS, such as smaller leakage current, steeper sub-threshold slope, higher packing density, weaker short channel effects, and smaller parasitic capacitances, etc [4]. The BOX in SOI however introduces a thermal barrier that enhances self-heating effects because of the low thermal conductive oxide. As a result, the average device temperature is substantially raised. In addition, due to the thin silicon island used as the active device region, large temperature gradients are observed in the silicon island and high peak junction temperature is induced. These reduce carrier saturation velocity and mobility and degrade device reliability and electronic characteristics. The higher device temperature also leads to stronger heat flow to interconnects and higher interconnect temperature, which increases the interconnect failure rate, delay time, joule heating and power consumption, etc [5].

Smaller MOSFETs are desirable for several reasons. One of the main reasons is to reduce the transit time for electrons/holes traveling from the source to the drain, which leads to smaller delay time (thus a higher clock rate can be used) for digital application and higher operating frequency for analog application. The other reason to make transistors smaller is to pack more and more devices in a given chip area. This results in a chip with the same functionality in a smaller area. Also, the cost per integrated circuits is mainly related to the number of chips that can be produced per wafer. Hence, smaller ICs allow more chips per wafer, reducing the price per chip. The transistor channel length has been constantly decreased over the years. The main problems that this reduction of channel length causes are the short-channel effects. These undesirable phenomena are caused by the fact that gate control over the channel is reduced by the influence of the drain potential. The most obvious result of this situation is that threshold voltage becomes dependent on channel length [6]. Another short channel effect is associated with interaction between the source-channel barrier and drain potential. In long-channel devices this barrier is controlled by the gate. As the channel length is decreased, the drain potential affects the barrier, making threshold voltage dependent also on drain bias. Finally, as source and drain get closer the risk of punch-through increases. A different problem resulting from the reduction of the device size is the power density produced in a single chip drastically increases because the number of devices increases. This also enhances the self-heating problems which leads to higher device temperatures and higher interconnect temperatures.

With the SOI CMOS transistor channel length currently being below 25nm [7], the undesirable short channel effects present themselves as extremely detrimental issues. One of the solutions to these short channel effects comes in the form of 3 dimensional SOI CMOS structures. One of the leading novel types of these devices is known as FinFET technology, which is shown in Figure 2. The device channel is the middle part of the fin that is wrapped by the gate, which is a type of Tri-gated MOSFET. The fin under the gate is lightly doped. The rest of the silicon is doped with opposite polarity similar to a planar MOS. The smallest FinFET device dimensions we have found in the published literatures include a 10 nm gate length, and 12 nm fin width [8]. In FinFET devices, electrical potential throughout the channel is controlled by the gate-to-source and drain-to-source voltages. This is possible due to the proximity of gate control electrode to the
current conduction path between source and drain. These characteristics of the FinFET minimize the short channel effect. Conventional MOSFET manufacturing processes can also be used to fabricate FinFET. They provide better area efficiency, and the mobility of the carriers can be improved by using FinFET process in conjunction with the strained silicon process [8].

Even though FinFET devices are seen as the leading solution to CMOS scaling limitations beyond the 22 nm node due to their superior electrostatics, thermal management in these ultra-scaled structures is an increasing concern. The issue of heating is made worse due to materials with poor thermal conductivity and the physical confinement of the device geometries lead to increased self-heating resulting in performance and reliability degradation. As FinFET process technology and integration progresses rapidly, FinFET parameters are being optimized to maximize their performance. It is necessary to simultaneously develop accurate and fast electro thermal modeling and simulation capability for simultaneous evaluation of the impact of the thermal characteristics on these parameters, which in turn impact the reliability and electrical performance of FinFETs. Self-heating is already known to degrade the drain current in SOI and strained-Si devices by around 15% due to the presence of a BOX in SOI type devices or a SiGe graded layer in strained-Si devices that increases the thermal resistance of the device due to low thermal conductivity of these materials [8, 10]. In FinFETs, the problem increases manifolds due to the small and confined dimensions of the fin that reduce its thermal conductivity. Self-heating is also known to degrade oxide reliability of FinFET devices [11, 12].

2. Background

There has been very little work in the area of developing thermal models for the FinFET device. In [13], Seshadi Kolluri et al. achieved modeling of the self-heating in FinFETs that was accomplished by dividing the structure into regions and solving the heat transfer equations. The solutions from neighboring regions were coupled to obtain heat flux continuity and boundary conditions. In contrast from previous efforts to model heating in FinFET devices, Seshadi Kolluri et al. made use of the fact that the majority of heat loss is to the substrate, while previous efforts have assumed that the majority heat was lost to the contacts. A one-dimensional (1-D) heat equation was used to model the heat flow in the fin, while a two-dimensional(2-D) heat flow equation was used to model the lateral heat spread in the gate, source and drain regions. Values
extracted from finite element calculations were used to account for the heat spread through the BOX and passivation layers. The work in [13] demonstrated a quite reasonable level of accuracy and suggests that a more rigorous model can obtain an extremely high level of accuracy.

In [14] Swahn and Hassoun, focused on the electro-thermal sensitivity in FinFET devices. Even though the self-heating was characterized, the assumptions made about the heat flow in the device limit the accuracy. Swahn et al. developed a metric of characterizing device robustness against self-heating with an accurate description of how leakage current and mobility are affected by self-heating. An important finding was that the fin width and gate length contribute significantly to the maximum device temperature. Even though Swahn and Houssououn performed a comprehensive sensitivity analysis their thermal model is lacking. A more accurate thermal model coupled with the work in [14] would yield a device model capable of accurate predictions of the FinFET device behavior.

Even in the absence of substantial work done towards thermal modeling of FinFET devices, there have been significant studies on the thermal modeling of SOI MOSFETs [5, 8, 10, 15-17]. In [15] a physics-based analytical heat flow model was developed. The SOI film and channel thermal resistances were used to describe heat loss to the oxide and substrate. The silicon island of the device was divided into several uniform regions. 1-Dimensional analytical heat flow models were used in the Silicon film and a 2-Dimensional model was used in field oxide (FOX). Unlike the work in [8, 10], the model presented in [15] does not assume constant channel temperature. Their model was coupled with a SPICE circuit simulator to perform electro-thermal simulation of simple SOI current mirror structures and CMOS differential amplifier. When compared against finite element simulations a reasonably high accuracy was displayed. These findings are both encouraging and extremely important to this research because a very similar approach will be used in the thermal modeling of the FinFET.

Although the proposed thesis work on thermal modeling of FinFETs is based on the model developed in [15], there are still many differences between these 2 approaches. Modifications from the model presented in [15] will be made due to the difference in the structure between a FinFET and a SOI MOSFET, especially along the channel and gate. In addition, the approach in [15] is an analytical mathematical model that was implemented in MatLab, and when coupled with a SPICE simulator, it was necessary that the iterations between SPICE and Matlab be activated externally. The proposed work will be a circuit model approach that will allow seamless implementation of the FinFET thermal circuit model in the SPICE simulator to couple directly with the electrical model of FinFETs. This will offer an effective electro-thermal simulation tool to take into account self-heating in FinFET devices and circuits.
3. Thermal Circuit Model for FinFETs

The proposed thesis work includes development of a thermal circuit for FinFET structure, accounting for non-isothermal effects along the fin, and implementation of the thermal circuit in a circuit simulator, such as Spice, for efficient and accurate electro-thermal simulation. Eventually, the electro-thermal simulation of FinFETs will be performed, and the thermal solution will be validated against finite element simulation. These are briefly discussed below.

![Figure 3](image)

Figure 3 shows a 2-D cross section of the FinFET from the source via the channel to the drain. The dash lines divide the film into six uniform regions for constructing the thermal circuit. The gate is supposed to wrap 3 sides of the channel, including top, front and back sides, as illustrated in Figure 2. For clarification of region divisions, only the top gate is shown.

3.1 Heat flow along the source, drain and fin

The first step requires solving the analytical thermal solution in each region on the silicon island, including the active device regions wrapped by the gate, the fin regions between the source/drain and the channel, and the source and drain contact regions. The metal contact on top of the large source/drain region shown in Figure 3 is not included in Figure 2. The heat flow along the silicon island needs to be determined, which will provide the accurate thermal profile along the island. The profile is needed to provide more accurate heat flow to the interconnects and the poly gate, which is crucial for prediction of interconnect temperature and thermal coupling between nearby devices. The analytical solution will then be converted into thermal circuit for the FinFETs. Implementation of the thermal circuit will allow channel temperature coupled with electrical model of the FinFET for self-consistent electro-thermal simulation.

Similar to [13, 15], in order to model the heat flow through the FinFET, the island is divided into uniform regions as shown in Figure 3. To account for the generated power, which is located in the channel-drain junction, the island is divided such that the power input is at the channel-drain junction which is the division boundary of Regions 3 and 4. The temperature of the portions of the source and drain regions under the metal contacts (Regions 1 and 6) can be assumed to be approximately constant because metal has a very high thermal conductivity. Therefore it is only
necessary to solve the heat equation in 4 regions; i.e., Regions 2-5 shown in Figure 3. Regions 1 and 6 can then be taken as thermal nodes.

Once the uniform regions are selected in the FinFET device, 2 boundary conditions (BC’s) for each interface between adjacent regions are needed to obtain analytical solution, including temperature and heat flux continuities at the interface. The analogy of these BC’s is the voltage and current continuities at the node that connects the circuit elements. This may include a current source that provides a current flowing into the node. The analogy is explained in detail in [15]. This is similar to a power source in the thermal flow problem, such as the generated power at the interface between Regions 3 and 4 in Figure 3.

Because of the thin island structure, temperature vertical to the island surface can be assumed constant. Also, due to the uniform power generation along the device width direction, the problem of heat flow along the thin island is reduced to a 1D problem if the heat flow out of the island is treated as losses that can be described by constant characteristic thermal lengths due to different heat loss paths. The simplified 1D problem can be described by the heat flow equation written as follows.

\[ \text{For regions 2 and 5,} \]
\[ \lambda_{\text{BOX}} \frac{dT_s}{ds} = -q_{\text{loss}} \]  \hspace{1cm} (1)

\[ \text{For regions 3 and 4.} \]
\[ \lambda_g \frac{dT_s}{ds} = -q_{\text{loss}} \]  \hspace{1cm} (2)

where \( \lambda_{\text{BOX}} \) and \( \lambda_g \) are the characteristic thermal lengths describing heat losses to BOX and the gate terminal, respectively and are constant in each region. \( T_s \) is the temperature along in the silicon island (Regions 2 – 5), and \( T_g \) is the gate terminal temperatures. The reference temperature at the bottom of the substrate is taken as a thermal ground to simplify the equations.

To obtain the accurate temperature profile, a detailed numerical simulation is usually necessary. However, the heat flow equations in Eqs. (1) and (2) offer an approximation that can reasonably describe the temperature distribution in the silicon island if the thermal lengths can be accurately determined. In this project, the thermal lengths will be studied and determined in terms of thermal resistances of the SOI structure and its terminals that will be extracted from a finite element simulation.

### 3.2 Thermal circuit for the FinFETs and electro-thermal simulation

Once the solution in each region is obtained in terms of the thermal resistance, a thermal circuit can be derived for the FinFETs. The thermal circuit can be implemented in a Spice simulator to solve the temperature profile in the devices. The circuit model can also be extended to multifinger FinFETs. In addition, the thermal circuit will be incorporated with the FinFET electrical model to perform electro-thermal simulation in Spice self-consistently with the FinFET electronic characteristics.
4. Future work

A basic FinFET structure will be first constructed in a finite element simulation environment, such as COMSOL or ANSYS. From these simulations the thermal resistances in different regions of FinFET will be extracted. The extracted values will be used as inputs, together with the material thermal properties and device dimensions, to the model described in Section 3. Afterwards finite element simulations will be used to verify the validity of the developed model.

Following the description presented in Section 3, a thermal circuit will be developed based on the analytical solution in each region of the FinFET structure. The developed circuit will then be incorporated with the FinFET device model for electro-thermal simulation. The model will be able to take into account the non-isothermal behavior of the FinFET device, and offers valuable information for chip designers to consider self-heating effects. The exiting thermal circuit in the FinFET model currently assumes constant device temperature and does not offer non-isothermal effect. This not only ignores the device peak temperature but it also inaccurately evaluates the heat flux to the interconnects. Both of these have crucial influences on device and interconnect reliability and must be carefully considered in chip design.

Although detailed numerical is able to offer accurate temperature profiles in devices to capture the device peak temperatures, any numerical simulation of FinFETs, including the finite element method, is very time consuming. As accurate as finite element simulations are, they become very impractical once we consider any common integrated circuits which require hundreds of thousands of transistors. In order to design any integrated circuit using the electrical model of devices, the information about the influence of its heating on electrical characteristics is very important. The proposed thermal circuit model is able to provide detailed heating information on FinFETs efficiently and accurate, and will offer an effective electro-thermal simulation tool for FinFET chip design.
## Timetable

<table>
<thead>
<tr>
<th>Month</th>
<th>Projected Task</th>
<th>Description</th>
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<tr>
<td>April</td>
<td>Thesis Proposal</td>
<td>Background research, description of the problem, learning the approach to solve the problem</td>
</tr>
<tr>
<td></td>
<td>Preliminary Research</td>
<td>Understanding the scope of the project, learning in-depth the fundamental concepts of the project, learning how to conduct the simulations and calculations, and constructing a basic FinFET structure in a 3D finite element package, such as COMSOL or ANSYS</td>
</tr>
<tr>
<td>May-July</td>
<td>Constructing thermal circuit model for FinFETs and validating the thermal circuit model</td>
<td>Submit progress report. Performing finite element simulations to extract thermal resistance needed for thermal model development, developing the thermal model for FinFETs, constructing thermal circuit and validating the developed thermal circuit with the finite element simulation</td>
</tr>
<tr>
<td>August</td>
<td>Electro-thermal simulation in Spice</td>
<td>Implementing the circuit model in Spice and perform electro-thermal simulation</td>
</tr>
<tr>
<td>September-October</td>
<td>Write research paper and submit a paper to IEEE</td>
<td>Work on a comprehensive research paper describing method and findings of research, submit the paper to IEEE Transaction on Electron Devices, prepare the thesis</td>
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<tr>
<td>November</td>
<td>Prepare the thesis</td>
<td>Prepare the thesis</td>
</tr>
<tr>
<td>December</td>
<td>Thesis Defense</td>
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References

[3] Extreme Design: Developing integrated circuits for -55 °C to +250 °C
[14] Swahn et. al Electro-Thermal Analysis of Multi-Fin Devices